Delayed Reset After Trip
Data Access Table gymnastics
Fri, Oct 14, 1994

The problem:

Detect a trip condition via a status bit, wait for maybe a few minutes, and apply a reset control action to recover from the trip. This note gives a concrete example of one method to do this via Data Access Table entries.

Solution:

Build a counter to count cycles since the start of a trip condition. Use a period specification entry conditioned by the counter value to enable the following reset control action, plus a clear of the counter channel in case the reset is not immediate, in order to insure that subsequent resets cannot occur too soon.

Example:

Suppose in node 056B, operating at 10 Hz, status Bit 0198=0 indicates a trip condition, channel 0013 is used as the counter channel, a delay of 5 minutes is required following a trip before resetting, and pulsing Bit 011C high for one 10Hz cycle resets a trip. (Use two non-volatile memory words at 40FF70 for constants. Set up the counter channel as a dummy settable channel so the clear works.) The following Data Access Table entries follow the approach outlined above:

```
1500   0013   0000   0000    Build cycle counter in Chan 0013 when Bit 0198 transitions
0000   8000   0198   0001    to zero.  Clear counter while Bit 0198 is one.


7F00   0001   0000   0000    Enable following entries when counter value falls outside
0000   C000   0013   0BB8    range 0000–0BB8. (0BB8 = 5*60*10 cycles)


0D95   0000   0040   FF70    Pulse Bit 011C high for one cycle.  (40FF70)=0401.
056B   011C   0000   0001


0D81   0000   0040   FF72    Clear counter to limit rep-rate of reset.  (40FF72)=0.
056B   0013   0000   0001    (Do this in case reset doesn't set Bit 0198 right away.)
```

If the reset pulse does not immediately cause Bit 0198 to become set, indicating a non-trip condition, then the last entry insures that the reset will only be done once. If the trip condition persists, and Bit 0198 continues to remain a zero, then the reset pulse will be re-issued 5 minutes later, when the counter again advances past BB8. If a reset occurs (manually) before the 5 minute timeout, the counter will be cleared.